IMPROVED INTEGRATED CIRCUIT STRUCTURE

ABSTRACT OF THE DISCLOSURE

A semiconductor chip carrier having an increased chip connector and plated through hole density. In particular, a substrate having a plurality of plated through holes therein, and a fatigue resistant redistribution layer thereon. The redistribution layer includes a plurality of vias selectively positioned over and contacting the plated through holes. The substrate further including a ground plane, two pair of signal planes, and two pair of power planes, wherein the second pair of power planes are located directly underneath the external dielectric layer. A buried plated through hole within the substrate.